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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/703,387	11/06/2003	Juanita DeLoach	TI-35862 (032350.B534)	9996

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EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 07/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/703,387	DELOACH ET AL.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-12 and 16-20* is/are rejected.

7)☒ Claim(s) *4-6 and 13-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/06/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is a first Office action on the merits of Application Serial No. 10/703,387. Currently, claims 1-20 are pending.

Election/Restrictions

2. The instant application contains two claimed inventions: I. claims 1-9 drawn to a method of forming a semiconductor device, classified in class 438, subclass 424; and II. claims 10-20 drawn to a semiconductor device (product-by-process), classified in class 257, subclass 501.

3. Since the inventions as claimed are cannot support separate patents and are not patentably distinct, a restriction requirement is improper at this time (see MPEP §803 - page 800-3 to page 800-4). However, the examiner reserves the right to make a restriction requirement if at any time during the prosecution of this application it should become necessary to do so (see MPEP §811 – page 800-54).

Specification

4. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. *Claims 1, 2, 7, 10, 11, 16, and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Choi (US 6,723,617 B1).*

5.1 The Choi patent (Choi) discloses a method for forming a semiconductor structure in manufacturing a semiconductor device, and a semiconductor device formed by the method (figs. 2A-2E and accompanying text). The method comprises the steps of: providing a pad layer 12 on a surface of a substrate 10 (fig. 2A and col. 3, lines 5-20); providing a nitride layer 14 on the pad layer (fig. 2A and col. 3, lines 24-37); providing a sacrificial oxide layer 16 on the nitride layer (fig. 2A and col. 3, lines 38-48); in a first etching step, etching at least the sacrificial oxide and nitride layers to define opposing substantially vertical surfaces of at least the sacrificial oxide and nitride layers (fig. 2C); in a second etching step, etching the nitride layer such that the opposing substantially vertical surfaces of the nitride layer are recessed from the opposing substantially vertical surfaces of the sacrificial oxide layer (fig. 2D); and in a

third etching step, etching the substrate to from a trench 30 extending into the substrate for purposes of defining one or more isolation regions adjacent the trench (fig. 2E).

5.2 The nitride layer comprises silicon nitride (col. 3, lines 24-37).

5.3 The nitride layer is wet etched using a phosphoric acid (col. 4, lines 16-20).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. *Claims 3 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi in view of Nagatani et al. (US 6,716,718 B2).*

6.1 Choi lacks anticipation in not teaching that the first etching step comprises etching the pad oxide layer, in addition to etching the sacrificial oxide and nitride layers.

6.2 The Nagatani et al. patent (Nagatani) discloses a method for forming a semiconductor structure in manufacturing a semiconductor device, the method being compatible with Choi (figs. 1, 15-17, and accompanying text). The method comprises the steps of: in a first etching step, etching a pad oxide layer 2, in addition to etching a silicon nitride layer 4 and a polysilicon layer 4 to

define opposing substantially vertical surfaces of the silicon nitride, polysilicon, and pad oxide layers (fig. 15, col. 4, lines 40-53, and col. 6, lines 43-47); in a second etching step, etching the polysilicon layer such that the opposing substantially vertical surfaces of the nitride layer are recessed from the opposing substantially vertical surfaces of the silicon nitride layer and the pad oxide layer (fig. 16 and col. 6, lines 48-50); and in a third etching step, etching a substrate 1 to from a trench 6 extending into the substrate (fig. 17 and col. 6, lines 57-60).

6.3 Choi uses three etching steps to form an etching mask which comprises pad oxide layer 12, recessed nitride layer 14, and sacrificial oxide layer 16 (fig. 2E). In the first etching step, the sacrificial oxide and nitride layers are etched to define opposing substantially vertical surfaces as shown in fig. 2C. In the second etching step, the nitride layer is etched such that the opposing substantially vertical surfaces of the nitride layer are recessed from the opposing substantially vertical surfaces of the sacrificial oxide layer as shown in fig. 2D. In the third etching step, the pad oxide layer 12 is etched (col. 4, lines 53-55). The resulting etching mask is subsequently used to etch the substrate 10, thereby forming trench 30 in the substrate (col. 4, lines 55-57). The patterned etching mask formed by Nagatani's etching sequence as shown in fig. 17 and the patterned etching mask formed by Choi's etching sequence are identical. However, Nagatani's etching sequence requires only two etching steps as compared with Choi's etching sequence, which requires three etching

steps. In other words, Nagatani's etching sequence forms the same patterned etching mask, but in fewer steps. Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Choi in view of Nagatani, by etching the pad oxide layer in the first etching step, in addition to etching the sacrificial oxide and nitride layers, as suggested by Nagatani, because in doing so the number of etching steps required to form the patterned etching mask is reduced.

7. *Claims 8, 9, 17, 18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi in view of Tseng (US 6,355,538 B1).*

7.1 Choi lacks anticipation in not teaching that the second etching step to recess the nitride layer comprises dry etching the silicon nitride layer using a plasma etcher, or that the entire method is performed in the plasma etcher without removing the structure from the plasma etcher.

7.2 Tseng discloses a method for forming a semiconductor structure in manufacturing a semiconductor device, the method being compatible with Choi (figs. 2-4 and accompanying text). The method comprises etching a nitride layer 22 in such that the opposing substantially vertical surfaces of the nitride layer are recessed from the opposing substantially vertical surfaces of a photoresist layer 24, as shown in fig. 3. The nitride layer is recessed using either a plasma etching process or a chemical wet etch (col. 4, lines 26-35).

7.3 It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to recess the nitride layer by a dry etching process

using a plasma etcher instead of by a wet etching process using a chemical such as phosphoric acid because, as taught by Tseng, both the dry etching plasma process and the chemical wet etching process are art-recognized isotropic etching techniques, i.e. both are used to perform lateral etching.

7.4 While Tseng teaches an isotropic dry etching plasma process to recess the nitride layer, Tseng does not teach that the entire method is performed in the plasma etcher without removing the semiconductor structure from the plasma etcher. Choi uses an anisotropic dry etching process to perform the first and third etching steps. This is evidenced by the opposing substantially vertical surfaces of the sacrificial and pad oxide layers (fig 2E). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Choi and Tseng by performing the entire method in a plasma etcher, since a plasma etcher is suitable for carrying out both isotropic and anisotropic dry-etching techniques.

Allowable Subject Matter

8. *Claims 4-6 and 13-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.* The prior art of record does not anticipate, teach or suggest - either separately or combined – a first etching step substantially as claimed which further comprises etching a portion of the substrate, as recited in claims 4 and 13. Also, the prior art of record does not anticipate, teach or suggest - either separately or combined – a

step of etching a portion of the substrate subsequent to the second etching step and prior to the third etching step, as recited in claims 6 and 15.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday-Thursday from 8:30 a.m. to 5:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TMT
26 June 2004

Mary Wilczewski
Primary Examiner